CLAIMS

What is claimed is:

1. A method for manufacturing multi-layer electronic devices, said method comprising the steps of:

providing a first device layer with a first series of resistive/conductive patterns thereon;

providing a second device layer with a plurality of via drilled therethrough;

bonding said first and said second device layers together to form a unitary body, wherein each of said via correspond to a respective capture pad in said first series of resistive/conductive patterns;

providing a second series of resistive/conductive patterns on an outer layer of said unitary body;

providing a plurality of terminations on said unitary body for electrical connection to other electronic devices;

inserting individual passive components vertically into each of said plurality of via;

bonding each of said passive components to its respective capture pad;

filling said via with a non-conductive material; and

forming electrical connections between each of said passive components and at least a portion of said second resistive/conductive patterns on said outer surface of said unitary device body.

2. The method of claim 1, wherein said first and said second device layers are made of FR4.

3. The method of claim 2, wherein said device is a printed circuit board.

4. The method of claim 1, wherein said first and second device layers are made of a non-conductive ceramic.

5. The method of claim 4, wherein said device is an integrated passive device.

6. The method of either claim 3 or 4, wherein the method of bonding said first and said second device layers is selected from the group consisting of: lamination, weight-firing, gluing or spritzing solvent.

7. The method of claim 1, further comprising, prior to providing said plurality of terminations, the steps of:

firing said device body to cure said second series of resistive/conductive patterns; and

trimming said second series of resistive/conductive patterns to achieve predefined component values.

8. The method of claim 1, wherein said passive components comprise any combination of resistors, capacitors, varistors, and thermistors.

9. The method of claim 8, wherein said passive components are bonded to their respective capture pads by way of solder reflow.

10. The method of claim 8, wherein said passive components are bonded to their respective capture pads by way of cured conductive epoxy.

11. A method for manufacturing multi-layer electronic devices, said method comprising the steps of:

providing a first device layer with at least one ground plane thereon;

providing a second device layer with a plurality of via drilled therethrough;

bonding said first and said second device layers together to form a unitary body, wherein each of said via correspond to a respective capture pad in electrical connection with said at least one ground plane;

providing a series of resistive/conductive patterns on an outer layer of said unitary body;

providing a plurality of terminations on said unitary body for electrical connection to other electronic devices, said at least one ground plane being in electrical communication with at least one of said terminations;

inserting individual passive components vertically into each of said plurality of via;

bonding each of said passive components to its respective capture pad; and

forming upper lands between each of said passive components and at least a portion of said resistive/conductive patterns on said outer surface of said unitary device body.

12. The method of claim 11, wherein said first and said second device layers are made of FR4.

13. The method of claim 12, wherein said device is a printed circuit board.

14. The method of claim 11, wherein the method of bonding said first and said second device layers is selected from the group consisting of: lamination, weight-firing, gluing or spritzing solvent.

15. The method of claim 11, further comprising, prior to providing said plurality of terminations, the steps of:

firing said device body to cure said second series of resistive/conductive patterns; and

trimming said second series of resistive/conductive patterns to achieve predefined component values.

16. The method of claim 11, wherein said passive components comprise any combination of resistors, capacitors, varistors, and thermistors.

17. The method of claim 16, wherein said passive components are bonded to their respective capture pads by way of solder reflow.

18. The method of claim 16, wherein said passive components are bonded to their respective capture pads by way of cured conductive epoxy.

19. A multi-layer electronic device comprising:

a first device layer with a first series of resistive/conductive patterns thereon;

a second device layer with a plurality of via drilled therethrough;

a unitary device body formed by the bonded union of the first and second device layers, wherein each of said via correspond to a respective capture pad in said first series of resistive/conductive patterns;

a second series of resistive/conductive patterns on an outer layer of said unitary body;

a plurality of terminations on said unitary body for electrical connection between other electronic devices and components of said device;

individual passive components vertically mounted into each of said plurality of via and bonded to its respective capture pad; and

an electrical connection between each of said passive components and at least a portion of said second series of resistive/conductive patterns on said outer surface of said unitary device body.

20. The multi-layer electrical device of claim 19, wherein said first and second layers are made of FR4.

21. The multi-layer electrical device of claim 20, where said device is a printed circuit board.

22. The multi-layer electrical device of claim 19, wherein said first and second layers are made of a non-conductive ceramic.

23. The multi-layer electrical device of claim 23, wherein said device is an integrated passive component.

24. The multi-layer electrical device of claim 19, wherein said passive components comprise any combination of resistors, capacitors, varistors, and thermistors.

25. A multi-layer electronic device comprising:

a plurality of first device layers, each such layer having a first series of resistive/conductive patterns thereon and a plurality of via drilled therethrough;

a plurality of second device layers, each such layer having a plurality of via drilled therethrough;

a unitary device body formed by the bonded union of an interleaved stack of said plurality of first and said second device layers, wherein each of said via correspond to a respective portion of the resistive/conductive patterns on the underlying device layer and wherein one of said second device layers forms the uppermost device layer and the lowermost device layer is one of said first device layers;

a second series of resistive/conductive patterns on an outer layer of said uppermost device layer;

a plurality of terminations on said unitary body for electrical connection between other electronic devices and various of the resistive/conductive patterns throughout said unitary device body;

individual passive components vertically mounted into each of said plurality of via and electrically connected to a portion of said underlying first device layer's first series of resistive/conductive patterns; and

an electrical connection between each of said passive components and at least a portion of said overlying first device layer's first series of resistive/conductive patterns through a corresponding one of said first device layer's plurality of via.